Amendments to the Claims

The following listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for collecting memory failure information in real time while performing a test of memory embedded in a circuit, comprising, for each column or row of a memory under test, the steps of:

~~for each column or row of a memory under test~~:

a. successively conducting uninterrupted testing of each memory location of said column or row according to a memory test algorithm under control of a first clock;

b. selectively generating a failure summary on-circuit while continuing to performing said uninterrupted testing of each memory location of said column or row; and

c. transferring off-circuit said failure summary from said circuit under control of a second clock concurrently with uninterrupted testing of ~~the~~ a next column or row in sequence.

2. (Currently amended) A method as defined in claim 1, step c. being initiated upon the later of completion of step a. in respect of said column or row and the completion of step c. in respect of a previous column or row ~~further including initiating said transferring said failure summary at the end of testing said column or row or at the end of transferring of an immediately preceding failure summary.~~

3. (Currently amended) A method as defined in claim ~~21~~, step a. being initiated upon the later of completion of step a. in respect of a previous column

or row and the initiation of step c. in respect of such previous column or row ~~further including delaying testing of such next column or row in sequence until said failure summary has been completely transferred off circuit.~~

4. (Currently amended) A method as defined in claim 1, wherein step c. comprises ~~further including performing said~~ transferring said failure summary during a transfer time substantially equal to ~~the~~ a time ~~required~~ to test a corresponding ~~row or~~ column or row.

5. (Currently amended) A method as defined in claim 4, wherein step b. comprises limiting said failure summary ~~having~~ to a bit length substantially equal to or less than said transfer time divided by ~~the~~ a period of said second clock.

6. (Currently amended) A method as defined in claim ~~5~~1, wherein step b. comprises the steps of:

i. if conducting uninterrupted testing of a column of the memory, ~~said generating a failure summary including~~ generating a column failure summary ~~having a first set of fields when said memory is accessed in column access mode~~ and if conducting uninterrupted testing of a row of the memory, generating a row failure summary ~~having a second set of fields when said memory is accessed in row access mode,~~ and

ii. generating a phase failure summary ~~having a third set of fields~~ upon completion of ~~a test phase~~the uninterrupted testing of said column or row.

7. (Cancelled).

8. (Currently amended) A method as defined in claim ~~1~~6, ~~each said failure summary comprising a combination of one or more of~~ wherein each of steps b.i and b.ii comprise: generating at least one ~~a~~ column or row failure address,

generating ~~one or more~~ at least one failure counts, and generating a failure mask ~~data~~.

9. (Currently amended) A method as defined in claim 8, wherein the step of generating at least one failure mask comprises recording ~~said failure mask data being~~ results of bit-wise comparisons between memory data outputs and expected memory data outputs.

10. (Currently amended) A method as defined in claim 1, wherein step b. comprises ~~said generating a failure summary further including~~ the steps of:

iii. classifying each detected failure according to predetermined failure types,

iv. maintaining a count of the number of failures of each of said predetermined failure types, and

v. ~~including~~ recording the~~a~~ count of each said failure types in said failure summary.

11. (Currently amended) A method as defined in claim 10, wherein step b.iii. comprises identifying ~~said predetermined failure types including a~~ massive failure type indicative of a predetermined number of failures in adjacent locations in a word of said memory.

12. (Currently amended) A method as defined in claim 10, ~~said predetermined failure types including~~ wherein step b.iii. comprises identifying at least one non-massive failure type ~~including~~ selected from a group consisting of a single bit failure type and a multi-bit failure type.

13. (Currently amended) A method as defined in claim ~~12~~10, wherein step b. comprises the step of:

vi. recording a ~~said failure summary including the row or~~ column or row address of each of a first and last failure detected in said column or row, respectively~~, and a count of each said predetermined failure types~~.

14. (Currently amended) A method as defined in claim 81, wherein ~~said~~ step b. comprises ~~of generating a failure summary including~~ selecting failure summary content based on at least one factor selected from a group consisting of memory test phase and ~~/or~~ memory access mode.

15. (Currently amended) A method as defined in claim 10, wherein step b.vii. comprises maintaining a count of at least one predetermined failure type selected from a group consisting of ~~said generating a failure summary including one or more of counting the total number of~~ failed locations, ~~counting the number of~~ failed locations with massive failures, ~~counting the number of~~ failed locations with non-massive failures; ~~counting the number of~~ single-bit failures and ~~the number of~~ multi-bit failures ~~identified associated with said column or row under test~~.

16. (Currently amended) A method as defined in claim 1, wherein step b. comprises a step of:

vii. ~~said generating a failure summary including~~ concurrently generating at least two ~~or more~~ failure summaries corresponding to at least two groups of a predetermined number of memory outputs ~~and said transferring including shifting said two or more failure summaries from said circuit in parallel via respective circuit serial outputs~~.

17. (Currently amended) A method as defined in claim 16, wherein step b.x. comprises ~~said two or more failure summaries including~~ concurrently generating a failure summary for each of at least two ~~or more~~ memories tested in parallel.

18. (Currently amended) A method as defined in claim 16, wherein step b.x. comprises generating ~~said two or more failure summaries including~~ a failure summary for each of at least two ~~or more~~ sections of a memory.

19. (Currently amended) A method as defined in claim 1, wherein step b. comprises generating ~~said failure summary including~~ at least two failure summary fields associated with each of at least two ~~or more~~ corresponding segments of said column or row of said memory and generating a fields relating to the complete column or row.

20. (Currently amended) A method as defined in claim 1, wherein step b. comprises the step of:

viii. ~~said generating a failure summary including~~ encoding selected failure information.

21. (Currently amended) A method as defined in claim 20, wherein step b.xi. comprises~~said encoding selected failure information including~~ encoding failure counts of each of a set of predetermined failure types when a count of a failure type exceeds a predetermined value associated therewith.

22. (Currently amended) A method as defined in claim 21, wherein step b.viii. comprises encoding ~~said encoding including determining~~ a percentage of ~~the number of defective cells~~ memory locations in a column or row that have failed corresponding to a failure count of at least one of the set of predetermined failure types.

23. (Currently amended) A method as defined in claim 21, wherein step b. viii. comprises ~~said encoding selected failure information further including maintaining~~ encoding a count of ~~the number of errors~~failures in each of at least two ~~or more~~ groups of adjacent cells in said column or row ~~and including each said count in said failure summary~~.

24. (Currently amended) A method as defined in claim 20, wherein step b.xi. comprises ~~said encoding selected failure information including~~ encoding a failure mask ~~data~~.

25. (Currently amended) A method as defined in claim ~~20~~24, ~~said encoding selected failure information including providing~~wherein step b.xi. comprises encoding an index ~~to identify~~indicative of a failed bit position of a memory output ~~that failed together with a bit to indicate~~and an indicator of whether ~~a~~ the failure mask contains more than one failing bit.

26. (Currently amended) A method as defined in claim ~~1~~16, wherein ~~said generating a failure summary including, generating in parallel a separate failure summary for each of two or more groups of a predetermined number of memory outputs.~~step c. comprises shifting said at least two failure summaries off-circuit in parallel via corresponding serial outputs of said circuit.

27. (Currently amended) A method as defined in claim ~~2~~616, wherein step b.x. comprises generating ~~each said separate failure summary including~~ a first field ~~for~~ identifying a failing group, a second field ~~for~~ corresponding to a failure mask ~~data~~ of said failing group, and a third field ~~for~~ indicating whether the at least one ~~or more~~ other groups contains failures.

28. (Currently amended) A method as defined in claim 27, wherein step b.x. further comprises generating ~~said failure summary including~~ a flag field associated with each of the at least two groups ~~for~~ indicating whether ~~an adjacent~~ group adjacent thereto is also defective.

29. (Currently amended) A method as defined in claim 1, wherein step b. comprises generating ~~said failure summary including~~ a flag field associated with

a column or row address field of a failing cell ~~for~~ indicating whether ~~an adjacent~~ cell adjacent thereto is also defective.

30. (Cancelled).

31. (Currently amended) A method as defined in claim 1, wherein step b. comprises ~~said selectively generating a failure summary including~~ generating a failure summary only when conducting uninterrupted testing of a column of the memory ~~said algorithm is in a column access mode~~.

32. (Original) A method of collecting memory failure information in real time while performing a test of memory embedded in a circuit for memory test phases that use a column or a row access mode, comprising, for each memory column or row under test:

testing each memory location of said column or row according to a memory test algorithm under control of a first clock;

generating on-circuit a failure summary while testing said column or row, said generating a failure summary including, for each detected failure:

determining whether said detected failure is a massive failure or a non-massive failure; and, if said detected failure is a non-massive failure:

classifying said detected failure according to predetermined failure types; and

updating a failure mask register with results of comparisons of memory outputs and expected memory outputs;

incrementing a count of each detected failure type; and

storing the row or column address of the first and last failures in said column or row, respectively;

upon completion of testing of said column or row, selecting a failure summary data depending upon whether a column or row was tested; and

transferring said failure summary from said circuit under control of said second clock concurrently with testing of the next column or row in sequence.

33. (Original) A method as defined in claim 32, said failure summary having a bit length equal to or less than the time required to test a column or row of said memory divided by the period of a second clock.

34. (Original) A method as defined in claim 32, further including initiating said transferring said failure summary at the end of testing said column or row or at the end of transferring of an immediately preceding failure summary.

35. (Original) A method as defined in claim 34, further including delaying testing of the second next column or row in sequence until said failure summary has been completely transferred.

36. (Original) A method as defined in claim 32, further including performing said transferring said failure summary during a transfer time substantially equal to the time required to test a corresponding row or column.

37. (Original) A method as defined in claim 32, further including performing said transferring said failure summary during a transfer time equal to or less than the time required to test a corresponding row or column.

38. (Original) A method as defined in claim 32, each said failure summary comprising a combination of one or more of a column or row failure address, one or more failure counts, and failure mask data.

39. (Original) A method as defined in claim 32, said selectively generating a failure summary further including generating a column failure summary when said algorithm is in column access mode, generating a row failure summary when said algorithm is in row access mode, and, following completion of a test phase, generating a phase failure summary.

40. (Original) A method as defined in claim 32, said selectively generating a failure summary including generating a failure summary only when said algorithm is in a column access mode.

41. (Currently amended) A memory test controller for testing a memory in a circuit, comprising:

means for conducting testing of each memory location of a column or row of said memory according to a test algorithm under control of a first clock in uninterrupted fashion;

means for generating a failure summary while testing ~~a~~ the column or row of said memory; and

means for transferring said failure summary from said circuit via a circuit output under control of a second clock while testing ~~the~~ a next column or row, if any, of a memory under test.

42. (Original) A memory test controller as defined in claim 41, said means for generating a failure summary including a transfer register for storing failure summary data.

43. (Currently amended) A memory test controller as defined in claim 42, said transfer register having a maximum bit length equal to or less than ~~the~~ a time ~~required~~ to test a column or row of said memory divided by the period of said second clock.

44. (Currently amended) A memory test controller as defined in claim ~~42~~41, said means for generating a failure summary including means responsive to phase input signals and memory access mode signals for selecting failure data to insert into said failure summary.

45. (Original) A memory test controller as defined in claim 41, further including failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types.

46. (Original) A memory test controller as defined in claim 45, said means for generating a failure summary including a counter means for counting detected failures of each of said predetermined failure types.

47. (Currently amended) A memory test controller as defined in claim 41, said means for generating a failure summary including failure address registers for storing ~~the~~ a row or column address of a first and of a last failure, if any, of a column or row under test.

48. (Original) A memory test controller as defined in claim 41, further including a failure mask register for storing results of comparisons of memory data outputs against expected data outputs.

49. (Original) A memory test controller as defined in claim 41, further including means for encoding selected failure summary information.

50. (Currently amended) A memory test controller as defined in claim 49, said means for encoding selected failure information including means for encoding failure counts of each of at least one predetermined failure types when a count of a failure type exceeds a predetermined value.

51. (Original) A memory test controller as defined in claim 50, said means for encoding including means for determining a percentage of the number of defective cells in a column or row.

52. (Currently amended) A memory test controller as defined in claim 50, said means for encoding selected failure summary information further including

means for maintaining a count of the number of errors in each of at least two ~~or more~~ groups of adjacent cells in said column or row and including each said count in said failure summary.

53. (Original) A memory test controller as defined in claim 49, said means for encoding selected failure summary information including means for encoding failure mask data.

54. (Currently amended) A memory test controller as defined in claim 49, said means for encoding selected failure summary information including means for providing an index to identify a bit position of a memory output that failed and ~~a bit to indicate~~an indicator of whether a failure mask contains more than one failing bit.

55. (Currently amended) A memory test controller as defined in claim 41, said means for generating a failure summary including:

a failure type identification circuit for determining to which of a set of predetermined failure types ~~of~~ each detected failure corresponds;

a failure type counter for each of said predetermined failure type;

a failure mask register for storing results of bit-wise comparisons between each memory output and corresponding expected memory outputs;

failure address registers for storing ~~the~~ a row or column address of each of first and last failure in a column or row;

a failure summary selection circuit for determining ~~the~~ content of said failure summary, and

a failure summary transfer register for holding said failure summary and;

a circuit for controlling shifting of failure data into and out of said transfer register.

56. (Original) A memory test controller for testing memory in a circuit, comprising:

means for testing each memory location of a column or row of a memory under test according to a test algorithm under control of a first clock;

a failure summary generator for generating a failure summary while testing a column or row of said memory, including:

failure type identification means responsive to a failure mask for classifying detected failures according to predetermined failure types;

counter means responsive to outputs of said failure type identification means for counting failures of each said predetermined types;

failure address registers for storing the row or column address of first and last detected failures in a column or row under test; and

a failure mask register for storing a failure mask containing results of comparisons of memory data outputs against expected data outputs;

means responsive to phase input signals and memory access mode signals for selecting failure data to insert into said failure summary a failure summary transfer register having a bit length equal to or less than the time required to test a column or row of said memory divided by the period of said second clock; and

means for transferring said failure summary from said circuit via a circuit serial output under control of a second clock while testing the next column or row, if any, of a memory under test.